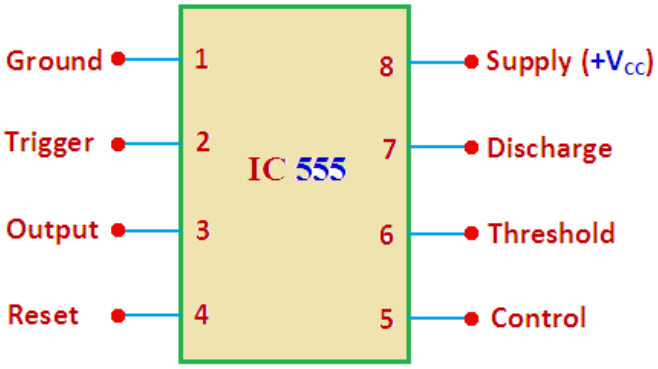
Principle of IC-555 Timer:

This is basically an IC chip which is essentially an integrated circuit and can be used conditionally as 'monostable' and 'astable' multivibrator. This is an indirect logic implementation of astable and monostable multivibrator where as the direct logic implementation of bistable multivibrator is SR Flip Flop.



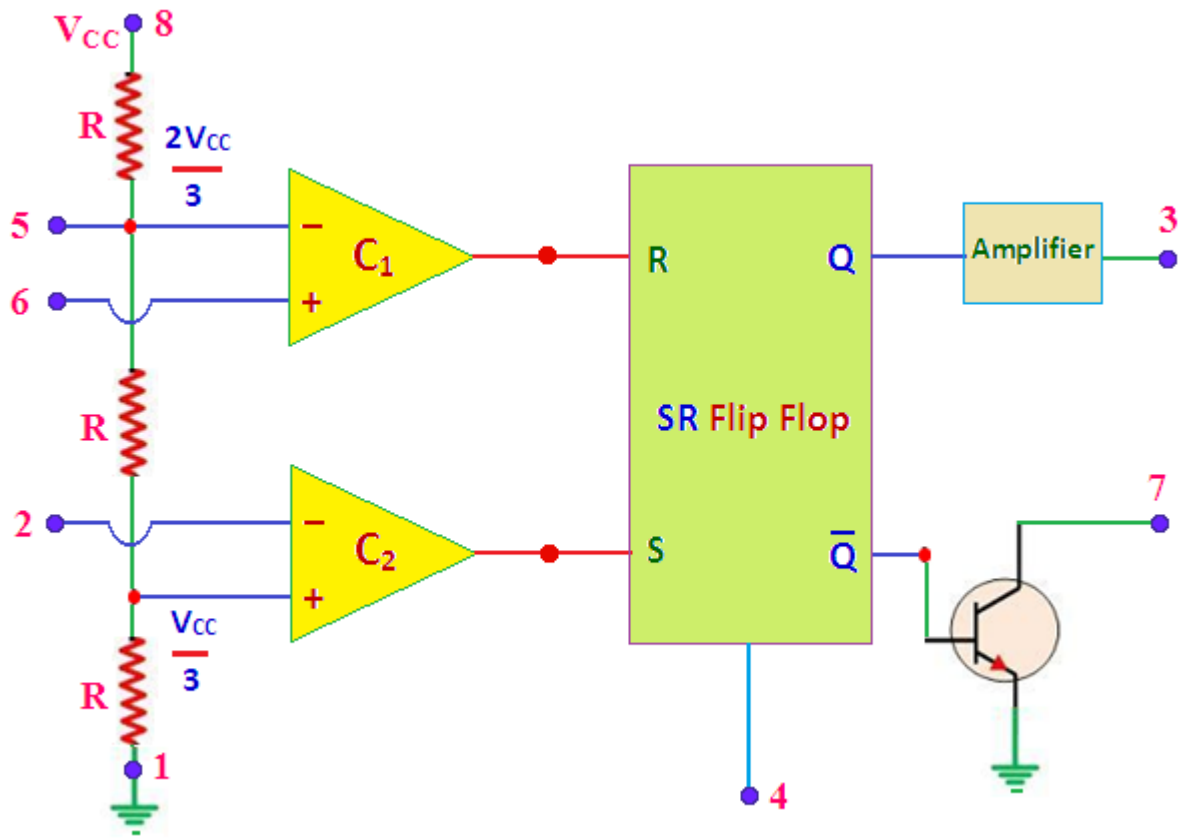
The basic circuit of this 'IC timer' is constructed by several digital analog components and the main active elements of the circuit of IC-555 are one SR Flip Flop, two OP-AMPS as two comparators, one n-p-n CE transistors and one potential divider with a power supply.

Here the pin configuration of this IC Timer is shown in figure. For this IC-555 timer there are 8 legs or terminals of this IC chip. The pin configurations are

1 – Ground, 2 – Trigger, 3 – Output, 4 – Reset, 5 – Control, 6 – Threshold, 7 – Discharge, 8 – Supply

Here for this IC-555, it has essentially two input terminals which are trigger input – 2 and threshold input – 6 and one output terminal – 3. The control terminal – 5 means that terminal at which certain fixed voltage should be supplied. Pin 1 or terminal – 1 should be made grounded and here reset terminal means the preset terminal of SR Flip Flop used. Also here supply means $+V_{CC}$ supply which should be given for the activation of this IC. And also the discharge terminal is the collector output of a transistor used.

Here in this IC-timer we used two OP-AMP as two comparators. Actually OP-AMP means operational amplifier which is basically a feedback amplifier and it is used for several mathematics operation. This OP-AMP is a differential or difference amplifier in which the output will be proportional to the difference of the voltages at its two input terminals. This OP-AMP has two input terminals which are inverting and non inverting input terminals.



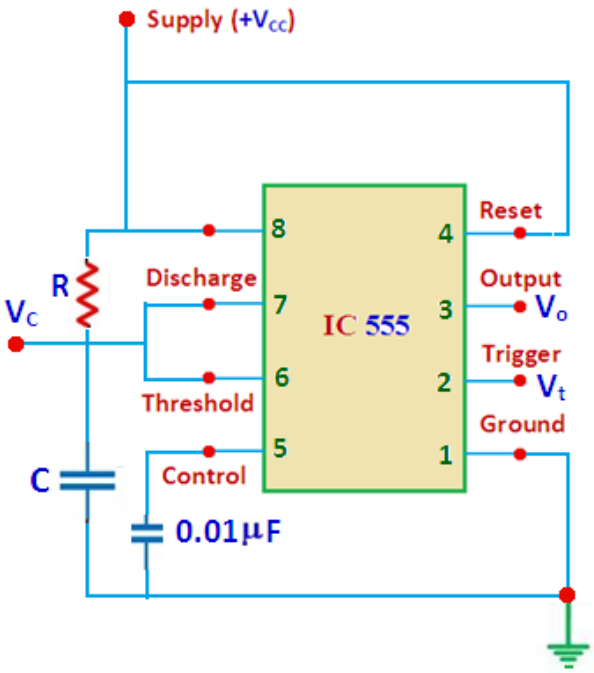
Here from the basic circuit diagram of this IC-555 timer as shown in figure, we see that two OP-AMPs are used as two comparators C_1 and C_2 where their outputs are connected with the input terminal of SR Flip Flop. For two input terminals which are trigger and threshold terminal, if the trigger voltage V_T given at trigger terminal – 2 which is less than $\frac{1}{3}V_{CC}$ then the output of comparator C_2 will be high and this leads to the input $S = 1$ of SR Flip Flop.

Otherwise output of C_2 will be low and this gives $S = 0$. On the other hand, if the threshold voltage V_{th} given to the threshold terminal – 6 be greater than $\frac{2}{3}V_{CC}$ then the output of comparator C_1 will be high and the leads to the input $R = 1$ of SR Flip Flop. Otherwise output of comparator C_1 will be low and this gives $R = 0$.

Application of IC-555 Timer as Monostable Multivibrator:

Here the necessary circuit diagram for using IC-555 timer as Monostable Multivibrator is shown in figure. At the beginning, let us consider that the SR Flip Flop of the main circuit is at Reset condition with $Q = 0, \bar{Q} = 1$. Thus at the beginning the output $Q = 0 = low$

Now if we supply the trigger voltage $V_t = V_{CC}$, the output of comparator C_2 will be low which gives $S = 0$ and we have still Reset condition $Q = 0, \bar{Q} = 1$ and output will remain low as before. In this case for $\bar{Q} = 1 = high$, the discharge transistor will become saturated and switched on.



At that time output voltage of terminal – 7 of discharge transistor will be low. And this makes the threshold voltage of terminal – 6 low. For this case the output of comparator C_1 will be low and this makes $R = 0$ with $S = 0$ and output of this SR Flip Flop will remain still at initial condition i.e. $Q = 0, \bar{Q} = 1$. This is basically the stable state of multivibrator.

If we now apply trigger voltage $V_t = low \left(< \frac{V_{CC}}{3}\right)$ then obviously the output of comparator C_2 will be high and this makes $S = 1$. This gives the output $Q = 1, \bar{Q} = 0$ and this is the set condition for which output voltage at terminal – 3 is high.

At this situation for $Q = 1, \bar{Q} = 0$ and discharge transistor will be in cut off condition with its output voltage at terminal – 7 is high. At that time capacitor C will start charging and with the continuation of charging of this capacitor, voltage across it will increase continuously and that voltage drop across that capacitor will be the effective voltage at threshold terminal – 6. With continuation of increment of this voltage when it exceeds $\frac{2}{3}V_{CC}$ at threshold terminal – 6, the output of comparator C_1 will be high which makes $R = 1$ and we get $Q = 0, \bar{Q} = 1$ which is our previous Reset stable state.

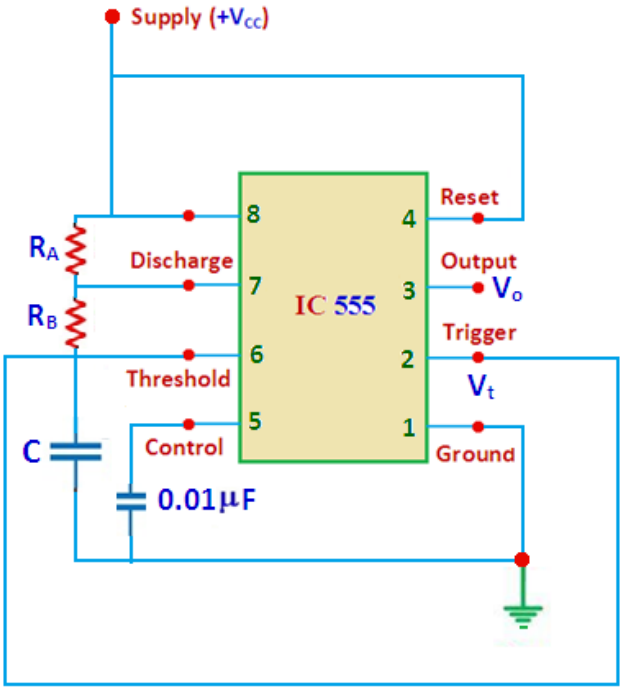
Thus for the whole operation of this circuit, this IC 555 behaves like monostable multivibrator with its one stable state $Q = 0, \bar{Q} = 1$ and another unstable state $Q = 1, \bar{Q} = 0$. By this manner, IC 555 timer will behave like Monostable Multivibrator.

Application of IC-555 Timer as Astable Multivibrator:

At the beginning of this IC timer as astable multivibrator (where necessary circuit diagram is shown in figure) the capacitor is uncharged and voltage across it is low which makes the trigger voltage at terminal – 2 low. For this case when it is less than $\frac{V_{CC}}{3}$ the output of

comparator C_2 will be high and this makes $S = 1$ and we get output $Q = 1, \bar{Q} = 0$ and output voltage of terminal – 3 will be high.

At that time with $\bar{Q} = 0$, the discharge transistor will be at cut off region (switched off) with voltage at terminal – 7 high. This makes capacitor C to start charging through the resistance R_B. With the continuation of the charging of the capacitor C, the voltage drop across it which is the effective voltage at threshold terminal – 6 will continue to increase. With this increment of voltage when this voltage at threshold terminal – 6 exceed $\frac{2}{3}V_{CC}$, the output of the comparator C_1 will be high. This makes $R = 1$ and we get output $Q = 0$ and $\bar{Q} = 1$.



With such $Q = 0, \bar{Q} = 1$, the discharge transistor will become saturated and will be switched on and its output voltage at terminal – 7 will be low. For this case the capacitor C will start to discharge and the voltage across it will continue to decrease. With such continuation of decrement of voltage across this capacitor when it reaches the value at trigger terminal – 2 less than $\frac{V_{CC}}{3}$, the output of comparator C_2 will be high and this makes $Q = 1, \bar{Q} = 0$. And we have reached the initial state and the process will be repeated.

Thus we see that with such operation of IC-timer the whole circuit behaves like an astable multivibrator having no stable state.